Dr. Babasaheb Ambedkar Open University
Term End Examination July – 2021

Course	:	BCA/DCA	Date	: 29-July-2021
Subject Code	:	BCAN-203(NEW)/DCA-203	Time	: 01:00pm to 03:00pm
Subject Name	:	Digital Electronics & Computer Organization	Duration	: 02 Hours
			Max. Marks	: 50

Section A

Answer the following (Attempt any two) (20)
1. Explain 9's complement and 10's complement
2. Explain 'binary coded decimal'.
3. Describe a working of ALU 74181
4. Describe a circuit diagram of DE Multiplexer

Section B

Answer the following (Attempt any three) (15)
1. Explain Binary Number System in detail.
2. $11001_2 = ?_{10}$
3. Explain Theorems governing Boolean Algebra
4. Explain 'Full Adder'.
5. Draw a circuit diagram for ' CLOCKED SET-RESET FLIP-FLOP'

Section C
Part – A (Multiple Choice Questions) (10)

1 In Boolean algebra, the OR operation is performed by which properties?
   A Associative properties   B Commutative properties
   C Distributive properties   D All of the Mentioned

2 The representation of octal number (532.2)8 in decimal is _____
   A (346.25)10   B (532.864)10
   C (340.67)10   D (531.668)10

3 According to Boolean law: A + 1 = ?
   A 1   B A
   C 0   D A'

4 The ALU gives the output of the operations and the output is stored in the _____
   A Memory Devices   B Registers
   C Flags   D Output Unit

5 The quantity of double word is _____
   A 16 bits   B 32 bits
   C 4 bits   D 8 bits

6 The weights used in Binary coded decimal code are:
   A 2,1   B 6,4,2,1
   C 8,4,2,1   D 4,2,1

7   Which of the following can be represented for decoder?

     A   Combinational circuit   B   Sequential circuit

     C   Logical circuit   D   None of the mentioned

8   The truth table for an S-R flip-flop has how many VALID entries?

     A   1   B   2

     C   3   D   4

9   Invalid BCD can be made to valid BCD by adding with _____

     A   0101   B   0111

     C   0110   D   1001

10   Which of the following is correct for a gated D-type flip-flop?

     A   The Q output is either SET or RESET as soon as the D input goes HIGH or LOW   B   The output complement follows the input when enabled

     C   Only one of the inputs can be HIGH at a time   D   The output toggles if one of the inputs is held HIGH

Part – B (Do as Directed)   (05)

State whether the following statement are True or False

1   A ripple counter is an asynchronous counter.

2   Bidirectional shift registers can shift data either right or left.

3   BCD arithmetic is performed using base 10 numbers.

4   The S-R flip-flop has no invalid or unused state.

5   Edge-triggered J-K flip-flops make it hard for design engineers to know when to accept input data.

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